REMARKS

Claims 1-10 are pending in the application.

Claims 1-10 have been rejected.

Claims 1, 2, 4-6, and 10 have been amended as set forth herein.

Claims 1-10 remain pending in this application.

Reconsideration of the claims is respectfully requested.

I. CLAIM OBJECTIONS

Claims 1 and 10 have been amended herein to correct informalities. Specifically, Claim 10 has been amended to replace "a-synclwonous" with "asynchronous" and Claim 1 has been amended to remove the phrase "at least" from line 13.

II. CLAIM REJECTIONS -- 35 U.S.C. § 112

Claim 10 was rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter. The November 14, 2008 Office Action states "*Claim 10 recites the limitation 'the signal value' in Line 11.*" The Applicant(s) have amended Claim 10 as shown above.

Accordingly, the Applicant respectfully requests the Examiner to withdraw the § 112 rejection.

III. CLAIM REJECTIONS -- 35 U.S.C. § 102

Claims 1-10 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,123,674 to *Mackey, et al.*, hereinafter "Mackey." This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-76 (8th ed., rev. 4, October 2005) (citing In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. Id. (citing

Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)).

Claim 1 comprises unique and novel elements, including those emphasized below:

> A circuit comprising a first and a second circuit module and a synchronization module the first and the second module being mutually a-synchronous, and being coupled by the synchronization module, the synchronization module comprising
>
> a transfer register for storing data which is communicated between the two circuit modules,
>
> a control circuit for controlling the register in response to a respective timing signal (St1, St2) from the first and the second circuit module, the control circuit comprising a control chain for generating a control signal (CR) for the transfer register the control chain including at least
>
> *- a repeater for inducing changes in the value of the control signal,*
>
> *- one edge sensitive element for delaying a change in the signal value until a transition in a selected one of the timing signals is detected.* (Emphasis Added)

The Applicant respectfully submits that the elements of Claim 1, including those elements emphasized above, are not taught, suggested, or anticipated by the art of record. Claim 1 recites the element, "a repeater for inducing changes in the value of the control signal". The Office Action indicates this element is anticipated by Fig. 4, element 415 of Mackey (Page 3, November 14, 2008 Office Action). The Applicant respectfully disagrees.

Element 415 is described by Mackey as follows:

> Source-enable signal 315 is produced by logic component 415, here an XOR gate positioned between the output Q of flip-flop 402b and the output Q of flip-flop 402c. *Accordingly, logic component 415 produces source-enable signal 315 for a full SCLK clock cycle when the output Q of flip-flop 402b is opposite the output Q of flip-flop 402c.* (Mackey, Col. 3 ll. 61-67.)

The Office Action has asserts that the "repeater" of Claim 1 is anticipated by the XOR gate of Mackey. As described in the section above, the XOR gate only produces an output when two flip-

flops are in opposition. This output is limited to a single high or low state based upon the state of the flip-flops connected to the XOR gate, and this output state is controlled by the logical exclusive disjunction operation preformed between the inputs. Therefore, the XOR gate of Mackey requires two inputs and further creates a signal that represents an exclusive disjunction operation between the two inputs.

It is respectfully submitted that the source-enabled signal 315 created by the XOR gate 415 of Mackey is not the same as the "repeater for inducing changes in the value of a control signal" as recited in Claim 1. The presently contemplated repeater, as illustrated in FIGURE 1 of the present application, has a single input (e.g., "a control signal"). It is respectfully submitted that the "repeater" of Claim 1 does not create a control signal from two inputs, but rather induces changes in the value of a control signal.

Moreover, rather than the exclusive disjunctive operation that is implied by the XOR gate, the repeater of the present disclosure may "amend[s] the value of control signal CR1" (Present Disclosure, Para [0023].) Such amending may be used to "obtain the second stage CR2" (*id*). An XOR gate performing a logical exclusive disjunctive operation would not be operable upon a single input, nor would it be able to amend a first value. Therefore, it is respectfully submitted that the "repeater" of Claim 1 is not taught, suggested, or anticipated by Mackey.

Claim 1 further recites, "one edge sensitive element for delaying a change in the signal value until a transition in a selected one of the timing signals is detected." The Office Action has indicates this element is anticipated by Fig. 4, element 415 of Mackey (Page 3, November 14, 2008). The Applicant also respectfully disagrees.

The Office Action has argued that flip-flops have an "inherent delay", and that this delay anticipates the delay of Claim 1. However, the Applicant respectfully points out that the "edge sensitive element" delays "until a transition in a selected one of the timing signals is detected." An inherent delay does not perform a delay until a signal is detected, rather only introduces an inherent delay that is irrespective of any signal being detected. Therefore, the "edge sensitive element" is not taught, suggested, or anticipated by the prior art of record.

Accordingly, the Applicant respectfully requests the Examiner to withdraw the § 102 rejection with respect to these claims.

IV. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining claims in the Application are in condition for allowance, and respectfully requests an early allowance of such claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***rmccutcheon@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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